2D electronics

https://doi.org/10.1038/s41565-025-02004-0

Deploying two-dimensional memristors on chip

Kaihui Liu

Two studies demonstrate wafer-scale synthesis of hexagonal boron nitride memristors compatible with CMOS technology and introduce opto-reconfigurable devices for broad-spectrum neuromorphic applications.

Among the candidate materials for next-generation memristors, hexagonal boron nitride (hBN), a two-dimensional (2D) insulator, has attracted considerable attention[1–3] because of its superior properties, including fast switching speeds, low operating voltages, high ON/OFF ratios, and exceptional thermal and mechanical stability[4–6]. In particular, hBN is well suited for integration into highly scaled devices. Nevertheless, practical adoption has been hindered by a critical obstacle: the growth of high-quality hBN films typically requires temperatures above 600 °C, which far exceed the thermal budget of standard silicon microelectronics[7,8]. As a result, hBN is often synthesized on foreign substrates and transferred onto target wafers — a process that introduces defects such as cracks, wrinkles, and contamination, which compromise device performance. Defects also hinder the seamless integration of hBN memristors with other functional components on-chip, limiting their applicability in complex systems. Now, two studies published in *Nature Nanotechnology* have demonstrated that this long-standing challenge can be overcome[9,10]. Both studies report wafer-scale synthesis of high-quality hBN memristors directly on a working substrate, without the need for high-temperature processing or post-growth transfer steps (Fig. 1).

Xie et al. developed a low-temperature plasma-enhanced chemical vapour deposition (PECVD) technique capable of growing vertically aligned hBN nanosheets at 330–360 °C, well within the back-end-of-line (BEOL) thermal budget of standard complementary metal-oxide-semiconductor (CMOS) fabrication[9]. By precisely tuning fluorine- and hydrogen-containing plasma chemistries, the researchers achieved uniform hBN films with thicknesses of 10–20 nm, directly integrated between metal electrodes on 1-inch silicon wafers. The resulting memristor arrays are fabricated without any transfer step and exhibit high device yield and performance.

In parallel, Chen et al. report an in situ PECVD growth process that enables the direct deposition of homogeneous hBN films on 4-inch silicon wafers at an even lower temperature of 250 °C (ref. 10). This advance allowed the fabrication of mixed-dimensional hBN/silicon heterostructure memristors, addressing the same integration barrier but with a focus on optoelectronic applications.

Beyond the achievement of wafer-scale device integration, the performance metrics of as-fabricated devices are impressive in both works.

According to the work of Xie et al., over 90% of devices demonstrated reliable non-volatile resistive switching — a notably high yield for 2D memristors. Each memristor could be incrementally programmed to more than 16 discrete conductance levels[9]. Such multi-level or analogue switching is essential for neuromorphic computing, as it allows a single device to emulate a range of synaptic weights, rather than being limited to binary states. Significantly, these analogue states are stable over time and exhibit minimal random telegraph noise, which is essential for maintaining computational accuracy in analog systems.

Xie et al. then integrated their memristors into a one-transistor-one-memristor (1T1M) configuration on a CMOS test chip. The integrated cells exhibit gradual, pulse-driven switching and maintain stable resistance levels over nearly one million cycles with minimal resistance drift. This level of endurance is comparable to that of commercial

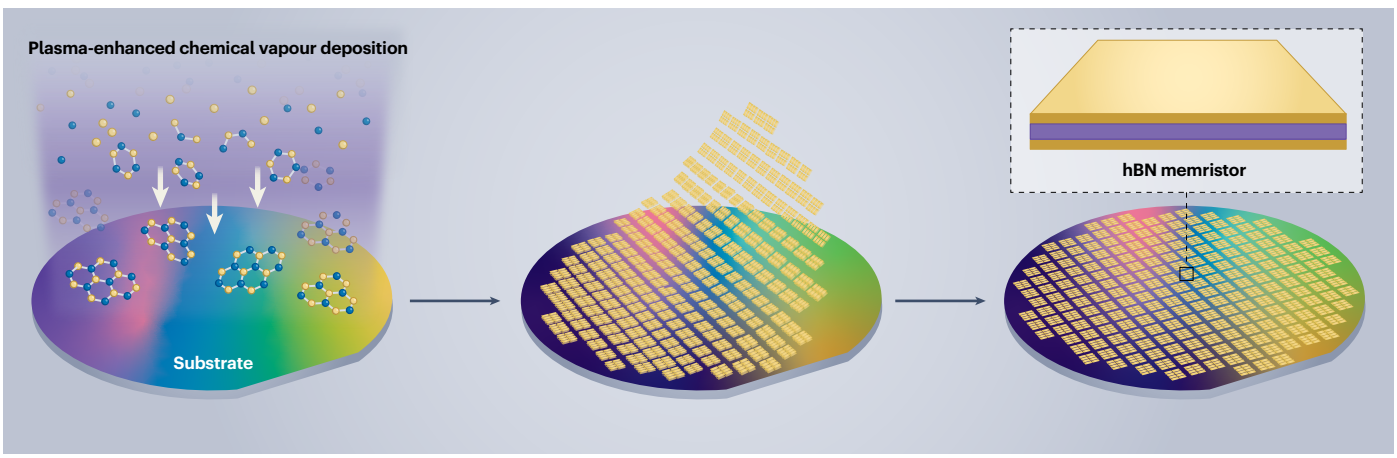

Fig. 1 | On-chip deployment of wafer-scale high-quality hBN memristors. Schematic illustration of the fabrication process for hBN memristors, depicting the plasma-enhanced chemical vapour deposition process for synthesizing hBN films and the device fabrication process for functional realization.

flash memory and the underlying transistors remained unaffected by the integration process. These results point to the feasibility of incorporating non-volatile memory directly into logic circuitry, which is a long-sought goal often described as 'CMOS+X' integration.

An additional advantage of direct hBN integration lies in the opportunity to introduce novel functionalities through clean and well-defined interfaces. The architecture proposed by Chen et al. allows for the hBN memristor to be constructed atop a silicon bottom electrode engineered to absorb light across a broad spectral range (375, 490, 595, 850, and 1,064 nm). The resulting photonic memristors operate in three distinct modes: a purely resistive mode with no memory, a volatile switching mode, and a non-volatile mode. This multi-modal behaviour, controllable via optical input, is both rare and powerful. It allows a single device to behave either as a long-term memory element or as a transient processing unit, depending on how it is stimulated. In essence, the same memristor can act as a stable synapse or a dynamic neuron in a neuromorphic circuit fully controlled by light.

This broadband, multifunctional operation is essential for artificial vision systems. In principle, each pixel in a vision chip could become an intelligent processing element, capable of filtering motion, adapting sensitivity, or performing in situ computation, without relying on external logic. The ability to toggle between volatile and non-volatile states means such pixels could emulate either stable synapses or dynamic, event-driven neurons, closely mimicking the visual preprocessing mechanisms found in biological eyes.

Collectively, the advances of Xie et al. and Chen et al. mark a turning point in the development of 2D devices. They demonstrate not only that wafer-scale integration of hBN memristors is technically feasible but also that such integration enables device performance and functionalities previously unattainable using traditional materials and methods. However, challenges remain for future applications of 2D memristors: ensuring high quality of 2D materials on full-wafer scales to achieve uniform performance of large-scale integrated devices, and verifying long-term reliability under realistic operating conditions (temperature variations, chip packaging, etc.), crucial for stability. As the field continues to evolve, next-generation intelligent hardware — such as neuromorphic accelerators, vision processors, and photonic co-processors, capable of learning and perceiving within a single chip — are poised to emerge in the near future.

Kaihui Liu [1,2] ✉

[1]State Key Laboratory for Mesoscopic Physics, School of Physics, Peking University, Beijing, China. [2]Songshan Lake Materials Laboratory, Dongguan, China.

✉e-mail: khliu@pku.edu.cn

Published online: 22 September 2025

References

1. Lanza, M. et al. *Science* **376**, eabj9979 (2022).
2. Zhu, K. et al. *Nature* **618**, 57–62 (2023).
3. Dean, C. et al. *Nat. Nanotechnol.* **5**, 722–726 (2010).
4. Kim, M. et al. *Nat. Electron.* **3**, 479–485 (2020).
5. Liu, Z. et al. *Nat. Commun.* **4**, 2541 (2013).
6. Shi, Y. et al. *Nat. Electron.* **1**, 458–465 (2018).
7. Wang, L. et al. *Nature* **570**, 91–95 (2019).
8. Wang, L. et al. *Nature* **629**, 74–79 (2024).
9. Xie, J. et al. *Nat. Nanotechnol.* https://doi.org/10.1038/s41565-025-01988-z (2025).
10. Chen, M. et al. *Nat. Nanotechnol.* https://doi.org/10.1038/s41565-025-01991-4 (2025).

Competing interests

The author declares no competing interests.